FILE 'HOME' ENTERED AT 09:32:16 ON 21 JUL 2005)

FILE 'INSPEC' ENTERED AT 09:32:38 ON 21 JUL 2005

L1	143	PERIPHER##### CIRCUIT
L2	170858	BOND#######
L3	47186	POROUS
L4	52766	(SWITCH##### OR DISPLAY)(P) CIRCUIT
L5	0	L1 AND L2 AND L3 AND L4
L6	36066	PERIP#######
L7	0	L6 AND L2 AND L3 AND L4
L8	0	L2 AND L3 AND L4
L9	23	L1 AND L4
L10	0	L2 AND L9

FILE 'CA' ENTERED AT 09:36:11 ON 21 JUL 2005

L11	0	L5
L12	36	L9
L13	0	L3 AND L12
L14	4	L12 AND L2

R 1 OF 4 CA COPYRIGHT 2005 ACS on STN
AN 142:269388 CA
ED Entered STN: 24 Mar 2005
TI Method for manufacturing liquid crystal display
IN Lee, Seong Hak
PA LG Philips LCD Co., Ltd., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
IC ICM G02F001-1337
CC 74-13 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	KR 2003094529	A	20031218	KR 2002-31227	20020604
PRAI	KR 2002-31227		20020604		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
KR 2003094529	ICM	G02F001-1337

AB A method for manufacturing a liquid crystal **display** is provided to reduce static electricity generated in a rubbing process, thereby preventing **peripheral circuit** part from being short. Alignment films are applied on active areas of an upper substrate and a lower substrate. Masks are placed on the upper substrate and the lower substrate, having the active areas as aperture parts. The aperture parts of the masks are rubbed. A seal pattern with an injection port is formed on the lower substrate. A plurality of spacers are scattered on the lower substrate. The upper substrate and the lower substrate are **bonded** with each other. The **bonded** upper substrate and the lower substrate are cut. Liquid crystal is injected between the upper substrate and the lower substrate through the injection port.
ST liq crystal display manuf alignment film rubbing process
IT Liquid crystal displays
(method for manufacturing liquid crystal display)

L14 ANSWER 2 OF 4 CA COPYRIGHT 2005 ACS on STN
AN 141:251544 CA
ED Entered STN: 30 Sep 2004
TI High resolution and brightness full-color led display manufactured using chemical-mechanical polishing technique
IN Dai, Yuan-Tung; Peng, Yuan-Ching; Chen, Chien-Chih
PA Industrial Technology Research Institute, Taiwan
SO Taiwan., 7 pp.
CODEN: TWXXA5
DT Patent
LA Chinese
IC ICM H01L033-00
CC 74-13 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
Section cross-reference(s): 73, 76
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	TW 486830	B	20020511	TW 2001-90102754	20010208
PRAI	TW 2001-90102754		20010208		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
TW 486830	ICM	H01L033-00

AB A full-color LED **display** consists of red, green, and blue LED elements. Red and green LED elements are formed on a first substrate and

covered by a first buffer layer. A second substrate is **bonded** to the buffer layer and polished to a thin substrate layer on which a blue LED element is formed. Then, a second buffer layer covers all three LED elements to form a full-color LED device. By arranging multiple full-color LED devices in rows and columns, and addressing and controlling each LED device by suitable wires, electrode layer and **peripheral circuit**, it is able to form a full-color LED **display** with high resolution and brightness.

ST full color electroluminescent display fabrication; polishing chem mech fabrication electroluminescent display

IT Polishing
(chemical-mech.; high resolution and brightness full-color LED display manufactured using chemical-mech. polishing technique)

IT Electroluminescent devices
Semiconductor device fabrication
Semiconductor electroluminescent devices
(high resolution and brightness full-color LED display manufactured using chemical-mech. polishing technique)

L14 ANSWER 3 OF 4 CA COPYRIGHT 2005 ACS on STN
AN 132:116202 CA
ED Entered STN: 18 Feb 2000
TI Manufacture of semiconductor memory devices
IN Inoue, Yoshihiko; Yoshioka, Hiroshi; Ureshino, Kazuhisa; Ohara, Kazuaki; Mishima, Michihiro
PA Hitachi, Ltd., Japan; Hitachi Super LSI System Co., Ltd.; Renesas Technology Corp.
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM H01L027-108
ICS H01L021-8242; H01L021-3205; H01L021-8234; H01L027-088; H01L027-10
CC 76-3 (Electric Phenomena)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000031415	A2	20000128	JP 1998-200276	19980715
	JP 3583927	B2	20041104		
PRAI	JP 1998-200276		19980715		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
JP 2000031415	ICM	H01L027-108
	ICS	H01L021-8242; H01L021-3205; H01L021-8234; H01L027-088; H01L027-10

AB Adjusting input/output capacitance value of the semiconductor device, to maximum and lowest standard or the request of the customer, adjust. Functions in the principal plane of semiconductor substrate as the component separation territory the formation to do thick silicone oxide film, 1st electrode the formation is done on silicone oxide film of the **peripheral circuit** territory. 1st electrode is formed simultaneously with the gate electrode of the MISFETs for memory cell selection. 1St and 2nd electrodes, which are actually semiconductor substrates, constitute, along with Si oxide insulator films, parallel-plate-type capacitors. The 1st electrode is connected to the **bonding** pad of 3rd interconnection layer. Selection of connection to **bonding** pads is carried out by the modification of the patterns of metal **switching** parts.

ST semiconductor memory device MIS FET

IT Electric capacitance
Semiconductor device fabrication
Semiconductor memory devices
(adjustment of input/output capacitance in manufacture of semiconductor

memory devices)
IT MISFET (transistors)
(manufacture of semiconductor memory devices)
IT 7631-86-9, Silica, uses
RL: DEV (Device component use); USES (Uses).
(adjustment of input/output capacitance in manufacture of semiconductor memory devices)

L14 ANSWER 4 OF 4 CA COPYRIGHT 2005 ACS on STN
AN 127:286007 CA
ED Entered STN: 11 Nov 1997
TI Active matrix type liquid crystal display device and its manufacture
IN Inoue, Shunsuke; Okita, Akira
PA Canon K. K., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
IC ICM G02F001-1343
ICS G02F001-136
CC 74-13 (Radiation Chemistry, Photochemistry, and Photographic and Other Reprographic Processes)
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 09244045	A2	19970919	JP 1996-56063	19960313
PRAI	JP 1996-56063		19960313		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
JP 09244045	ICM	G02F001-1343
	ICS	G02F001-136

AB In the liquid-crystal **display** device comprising a liquid-crystal layer enclosed between a substrate equipped with image **display** units containing a **switching** element and peripheral circuits for sending signals to the **display** units, and another substrate bearing a transparent electrode, an electrode layer of the type used for the pixel electrode in each **display** unit is also formed on the **bonding** pad of the **peripheral circuit**. Also claimed is a method for manufacturing the above liquid-crystal **display** device. The properties of the **switching** elements are improved.
ST active matrix liq crystal display; **bonding** pad liq crystal display
IT Liquid crystal displays
(active matrix type liquid crystal display device and its manufacture)

WEST Search History

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DATE: Thursday, July 21, 2005

Hide?	Set Name	Query	Hit Count
	DB=PGPB,USPT,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
☐	L59	L58 and l41	0
☐	L58	L57 and l56 and l51	54
☐	L57	switch$5 or display$5	4079269
☐	L56	switch$5 or display$5	4079269
☐	L55	perpher$5	1294
☐	L54	perpher$5	1294
☐	L53	l51 and l41	0
☐	L52	L51 and l44	0
☐	L51	L50 and l45	54
☐	L50	L49 and l48	54
☐	L49	tatsuya.inv.	47981
☐	L48	L47 and tft and l45	68
☐	L47	active adj matrix	41021
☐	L46	thin adj film	438646
☐	L45	shimoda.inv.	9524
☐	L44	bond$5 and l42	15
☐	L43	l5 and l42	1
☐	L42	L41 and l40	30
☐	L41	porous	432210
☐	L40	mulpuri.xa,xp.	598
☐	L39	l35 and l37	27
☐	L38	L37 and l4	0
☐	L37	hideo.asn.	3804
☐	L36	L35 and l4	7
☐	L35	sony.asn.	285376
☐	L34	l33 not l24	49
☐	L33	l32 not l30	56
☐	L32	L31 and l5	66
☐	L31	438/10-127.ccls.	34345
☐	L30	L29 and l5	44
☐	L29	438/455-465.ccls.	4843

☐	L28	438/455465.ccls.	0
☐	L27	l23 not l25	5
☐	L26	l24 not l23	135
☐	L25	L24 and l23	19
☐	L24	leedy.inv.	154
☐	L23	l12 and l19	24
☐	L22	L21 and l4	1254
☐	L21	mono and poly$5	185478
☐	L20	L19 and l15 and l16	2
☐	L19	L18 and l17	693
☐	L18	polycrystal$5	107174
☐	L17	(mono adj crystal$5) or mono-crystal$5	3232
☐	L16	display adj circuit	16158
☐	L15	peripher$5 adj circuit	28031
☐	L14	peripher45 adj circuit	0
☐	L13	L12 and l9	187
☐	L12	L11 and l5	557
☐	L11	257/$.ccls.	312967
☐	L10	257/$.ccls.	312967
☐	L9	L8 and l5	260
☐	L8	438/$.ccls.	169737
☐	L7	L6 and l5	129
☐	L6	349/$.ccls.	36771
☐	L5	peripher$5 and bond$5 and porous and display	5813
☐	L4	peripher$5 and bond$5 and porous and display	5813
☐	L3	perpher$5 and bond$5 and porous and display	3
☐	L2	porous and bond$5 and perpher$5 and display	3
☐	L1	display and porus and bond$5 and peripher$5	7

END OF SEARCH HISTORY